What is claimed is:

1. A liquid crystal display, comprising:

a gate driver driving gate lines on a liquid crystal display panel;

a timing controller controlling the gate driver; and

a masking part selectively intercepting a gate output enable signal corresponding to an abnormal state of a gate high voltage, wherein the gate output enable signal is supplied to the gate driver from the timing controller.

2. The liquid crystal display according to claim 1, wherein the masking part intercepts the gate output enable signal during an abnormal period when the gate high voltage drops below a designated voltage.

3. The liquid crystal display according to claim 1, wherein the masking part includes:

a detection part detecting an abnormal period of the gate high voltage to generate a gate voltage abnormality detection signal; and

a switching part switching the gate output enable signal and the gate voltage abnormality detection signal in accordance with the gate voltage abnormality detection signal.

4. The liquid crystal display according to claim 3, further comprising:

a period-extending part connected between the detection part and the switching part for further extending a period, during which the gate output enable signal is intercepted, by a designated period in use of the gate voltage abnormality detection signal.

5. The liquid crystal display according to claim 4, wherein the period-extending part delays the gate voltage abnormality detection signal for the designated period to supply the delayed gate voltage abnormality detection signal to the switching part.

6. The liquid crystal display according to claim 3, wherein the detection part includes:

a sensing part sensing a voltage level of the gate high voltage; and

a logical signal generator for generating the gate voltage abnormality detection signal with any one logical state of high state or low state in accordance with the voltage level of the sensed gate high voltage to supply the generated gate voltage abnormality detection signal to the switching part.

7. The liquid crystal display according to claim 2, further comprising:

a second masking part selectively intercepting the gate output enable signal supplied from the timing controller to the masking part, in accordance with a reset signal.

8. A driving method of a liquid crystal display, comprising the steps of:

generating a gate voltage abnormality detection signal corresponding to an abnormal state of a gate high voltage; and

selectively intercepting a gate output enable signal supplied from a timing controller to a gate driver in accordance with the gate voltage abnormality detection signal.

9. The driving method according to claim 8, wherein the gate output enable signal is intercepted during an abnormal period when the gate high voltage drops below a designated voltage, in the step of selectively intercepting the gate output enable signal.

10. The driving method according to claim 8, wherein the step of generating the gate voltage abnormality detection signal includes:

sensing a voltage level of the gate high voltage; and

generating the gate voltage abnormality detection signal with any one logical state of high state or low state in accordance with the sensed voltage level.

11. The driving method according to claim 8, further comprising the step of:

having the gate output enable signal further intercepted for a designated period in response to the gate voltage abnormality detection signal.

12. The driving method according to claim 8, wherein the gate output enable signal is

output to the gate driver if the gate high voltage is in a normal state and is intercepted if the gate high voltage is in an abnormal state during the step of selectively intercepting the gate output enable signal.